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Involved Partners: ABIX GmbH (ABI)  
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FZI Forschungszentrum Informatik (FZI)  
Infineon Technologies AG (IFX)  
Kasper & Oswald GmbH (KAOS)  
Noiseless Imaging Oy (NI)  
OFFIS (OFF)  
Robert Bosch GmbH (RB)  
SparxSystems CE (SSCE)  
Tampere University of Technology (TUT)  
Technische Universität München (TUM)  
Universität Paderborn (UPB)  
Visy Oy (VIS)

Deliverable Lead Partner: Universität Paderborn (UPB)

**Content**

<b>1</b>	<b>Introduction</b>	<b>3</b>
<b>2</b>	<b>State-of-the-Art Analysis</b>	<b>4</b>
2.1	Model-Driven Design	4
2.2	IoT Software Compilation and Optimization	5
2.3	Ultra-Low Power Software	6
2.4	IoT Security	7
2.5	IoT Operating Systems	8
2.6	GPU Code Generation and Optimization	9
2.7	IoT Analysis	10
<b>3</b>	<b>Related Projects</b>	<b>11</b>
<b>4</b>	<b>References</b>	<b>13</b>
<b>5</b>	<b>Appendix A - Table of Acronyms</b>	<b>18</b>

# 1 Introduction

The Internet-of-things (IoT) has the potential to improve our lives dramatically. The backbone of industry automation, smarter homes, higher energy efficiency, better health care, assistance of elderly people and more flexibility in working environments are only some areas that can be imagined today and realized tomorrow. The tremendous impact of IoT on our industrial environments and our private life is a key reason to consider IoT research and developments as important pillars in the European Horizon 2020. Impact to our private life are, for instance, in home automation via so-called IoT edge devices like smart light bulbs which are expected to come almost at the same costs as non IoT enabled devices in near future. Another rapidly evolving market is in industry automation (Industrial IoT), which is expected to grow dramatically for the next decade pushed by several initiatives like the German Industry 4.0 strategy.

IoT devices with sensors and actuators need electronics to connect that world of “things” with the digital world of the Internet. Yet software runs the IoT electronic device hardware. Since IoT devices need to be smart, cheap and capable to run with extremely small amounts of energy – known as ultra-thin IoT nodes – IoT software must also be ultra-thin with extremely small memory footprints and ultra-low energy consumption. At the same time, software must provide smart functions including real-time computing capabilities, connectivity, security, safety, and remote update mechanisms. Recent publications support the claim of ultra-thin – and low cost – IoT devices. So, for instance, Walmart calls for sub-1\$ IoT sensors [80] and ARM TechCON targets at sub-50cent IoT SoCs [81].

These constraints put a high pressure on IoT software development. Due to the very limited resources provided by IoT nodes, today’s commonly used design approach to trade-off development time with software efficiency is not competitive any longer. Therefore, an industry-wide effort in the course of the COMPACT project is needed to provide measures for fast and efficient IoT software development. The main goal of the COMPACT project is to provide novel solutions for the application-specific and customer-oriented realization of ultra-thin IoT nodes with focus on software generation for IoT devices with ultra-small memory footprints and ultra-low power consumption. To obtain this goal, COMPACT will create important technological innovations to automate the software development and configuration flow for ultra-constrained IoT nodes. As such, it can be seen as carefully developed software construction robots that will be developed in this project. The automation methodology follows the OMG notion of model-driven architecture (MDA) and applies it to the development of IoT device software. Due to the main principles of MDA, COMPACT will follow a scalable approach using carefully designed meta-models and generators for auto generating the required software as its key concept. In detail, the MDA-based flow and tool chain will be enabled by the new IoT Platform Modelling Language (IoT-PML), highly efficient analysis and optimization methods, and a reference IoT tooling framework.

The next chapter provides the current state-of-the-art in areas which are related to the research and development activities of the COMPACT project and list related R&D projects thereafter.

## 2 State-of-the-Art Analysis

### 2.1 Model-Driven Design

The Object Management Group (OMG), which adopted the UML as a standard, has developed a meta-modelling architecture to define the UML. This meta-modelling architecture enables the extension of the UML with so-called UML profiles. The standard UML profile for Modelling and Analysis of Real-Time and Embedded systems (MARTE) extends the UML with key notations (non-functional properties such as time and resources) for real-time computing. MARTE extends UML with the capability to model the hardware and software layers (middleware) and interconnections that compose an execution platform. Platform components can be described at the same level of abstraction as the application, and they may thus also contain timing information along with structural and behavioural aspects. The allocation model describes the mapping of application functions onto execution platform resources. This enables the optimisation of the software with regard to scheduling. However, for optimisation of the embedded software a more general specification of the hardware base line is required, and system level approaches are still insufficiently supported.

The Systems Modelling Language (SysML) on the other hand extends UML to offer support for modelling hardware (mechanical and electrical). The SysML extends the UML, to model hardware aspects such as parallelism, critical regions, or requirement modelling. The language is often used in the domain of systems engineering. It widens the UML focus towards software and enables the modelling of the complete system. It uses blocks to model the parts of the system, instead of classes as part of the software. On basis of the system view, SysML provides an interesting part in modelling the information basis for the generation of ultra-thin software. However, it still lacks aspects such as variability or a detailed conditional architectural specification.

Other UML profiles exist such as EAST-ADL2 or UPDM. All the UML profiles focus on dedicated system or software aspect. In the effort to create a comprehensive data basis for the generation of ultra-thin software for IoT devices these approaches have to be unified, and the required parts of each approach identified respectively.

State-of-the-art technology available in a powerful modelling tool like Enterprise Architect by SparxSystems (an OMG member) allows the implementation of a new modelling profile, approach and best practices that adheres to desired standards while at the same time extending capabilities beyond the current confines of UML to address IoT-specific requirements and effectively merge the heretofore segregated evolution of software, hardware and firmware.

When UML comes with code generation, it is typically based on the principles of the Model-Driven Architecture (MDA), which has provided significant advances in the design and analysis of embedded software throughout the last years [72]. By providing a domain-specific profile or meta-model, instead of the source code, MDA offers the benefit to support different generation processes and, therefore, to easily adjust to different scenarios or hardware base lines. The influence of the underlying hardware baseline is crucial for the quality of the design and the fulfilment of requirements in a model-based design process for embedded software, especially if a resource efficient ultra-thin design is targeted. Currently, Model-Driven Architecture (MDA) is applied to different, vertical domains based on different meta-models, UML profiles, languages, middleware and operating systems.

There has been various work and projects to bring model-driven architecture (MDA) principles to the IoT domain. One MDA tool is described in [30]. It offers a graphical domain-specific language for design entry and modelling and code generation facilities for IoT standards. It combines the different domain views on IoT communication, things and IDs as well as the processing of vast amounts of data. Another work in [31] describes a model-driven IoT flow focusing mainly on communication. They propose to specify functionality with IoT-specific DSL formats and map the specification on an automata-based platform independent meta-model. Code generators generate the platform-dependent code. The MDA tool proposed in [32] uses state transition diagrams as programming model for design and modelling IoT applications in a platform-independent way. Code generators produce the platform dependent code. For commercial solutions, code generation tools and the MDE design flow from MATLAB/Simulink is widely adopted in industry. [73]

introduces a SysML profile that addresses heterogeneity within a system of IoT devices and enables model-driven development of IoT applications. The profile is based on the IoT domain reference model introduced by the IoT-A project [74]. [75] introduces a model-based design process using the BIP component language [76] for the analysis of REST-based web services that integrate IoT devices. However, all do not fit the specific needs of very resource-constrained ultra-thin hardware platforms and the generation of efficient application software for such platforms.

Within the IoT domain, also variability of software and hardware platforms needs to be considered. A large number of variability modeling languages exists for different domains. Approaches like the Common Variability Language (CVL) [77], or feature diagrams, which have been introduced as part of the Feature-Oriented Domain Analysis (FODA) method [78], use graphical notations. Textual variability languages, such as Clafer [79], the INDENICA Variability Modeling Language (IVML) [80], or the Textual Variability Specification Language (VSL) [81] promise improved scalability with respect to model size and complexity over purely graphical variability modeling approaches.

Besides UML based approaches, other modelling approaches exist used by the industry. IP-XACT [67] is Accellera Systems Initiative's specification for documenting Intellectual Property (IPs) hardware designs. It enables highly automated design creation and configuration in a tool independent and machine-readable manner. Especially in the automotive domain the structural view at the hardware baseline level is needed to allow the automated import of IP-XACT components as well as the automated generation of virtual prototypes including multicore processors, peripheral devices, and reused IP blocks. While this is a detailed specification of the interfaces of IP and structural view of an IP-based design, it only contains very abstract inclusion of software aspects. Kactus2 [68] is an Open Source EDA tool for creating and editing IP-XACT designs. Kactus2 strictly follows the IP-XACT standard and provides RTL synthesis for targeting FPGA and ASIC designs.

ThingML [69] has been applied as a modelling language for embedded and distributed devices. ThingML focuses on the Internet of Things [8] domain and targets resource constrained embedded systems such as low power sensor and microcontroller based devices. There exists a model-driven software engineering tool-chain for ThingML, and code generators for various devices. Another widely adopted modelling language for embedded devices is the Architecture Analysis and Design Language (AADL) [27]. AADL targets at distributed computing systems with real-time requirements. It offers a device class suitable to describe IoT devices, yet it focuses mainly on their interaction not on the implementation. Thus, it also does not offer the capabilities required for ultra-thin code generation. Another model-based language focusing on data-flow oriented design is RVC-CAL defined in ISO Standard 23001-4:2011 [28]. RVC-CAL is a high-level data flow model-based language that can be considered similar to MATLAB/SIMULINK in the sense that it needs to be compiled/synthesized to C or Verilog for implementations. An open source compiler "Orcc" exists [29] and offers code generation to a variety of platforms. Code generation approaches from RVC-CAL to resource constrained devices do exist: a very recent work [70] generates multi-threaded C code that is not dependent on any external libraries, whereas [71] generates LLVM bytecode, however intended for a particular "TTA" (Transport Triggered Architecture) type processor architecture.

Yet, all these works may not capture all aspects required for efficient development and code generation of IoT devices. COMPACT will provide the high granularity and interlinked model styles, which are required on all levels from hardware over OS to SW and communication stacks to the IoT environment and scenario to design an ultra-thin IoT device to fulfil requirements on resource limitations, power, timing, safety and security.

## 2.2 IoT Software Compilation and Optimization

Memory was always a significant cost factor not only for ultra-thin devices throughout history of computing. Thus, there exists a broad range of research on techniques to reduce the memory footprint of software for the instruction code section, usually written to ROM, and the program's data section consisting of data, heap and stack, usually residing in RAM. These techniques are continuously driven by an increasing trend towards the incorporation of computers into a variety of compact embedded devices with limited amount of available memory.

A major class of memory minimization methods is based on compiler optimizations techniques, in order to reduce the size and increase the performance of applications [9]. Careful, aggressive, inter-procedural optimizations (IPOs) – so called whole-program analysis – take the entire application into account by applying IPOs at link time. Whole-program analysis increases optimization opportunities. Since the compiler has visibility over every function in every compilation unit, decisions that would normally use conservative estimates can instead be based on data-flow information crossing file boundaries. Link time optimization (LTO) techniques include a number of inter-procedural analyses, such as context-sensitive points-to analysis, call graph construction, Mod/Ref analysis, as well as code transformations and compactions like inlining, constant propagation, dead/unreachable/redundant code elimination. The LTOs in LLVM for example operate on the LLVM intermediate representation (IR) directly, taking advantage of the semantic information, it contains. At compile time, inter-procedural summaries can be computed for each function in the program and attached to the LLVM bytecode. The link time optimizer can then process these summaries as input and reduce program overhead in terms of code size, execution time or power consumption [10] [11]. GCC (since version 4.5) also supports LTOs for optimizing code size, code locality, and performance in real-world applications [12]. LTOs are not limited to a static analysis approach but can be refined using scenario-based application trace profiles for cross-module optimization. Profile Feed-back Based Lightweight IPO (LIPO) is a compiler cross-module optimization technique combining both IPO and Profile Guided Optimizations (PGO). LIPO sensitively enhances code visibility boundaries for optimization passes, where optimization decisions are derived from the profile collected by the application test run. Profile-driven optimization decisions can be a lot more precise and reliable because real scenario data is used instead of over-approximations and assumptions that are used by the compiler heuristics for static code analysis. Here, for example, hot and cold code sections are profiled. Hot code sections called often are optimized towards performance while cold code sections, such as exception handlers, which are called rarely, are optimized for code size.

Another approach to LTO is ThinLTO as available in the LLVM framework (as described in [84]) which is scalable and incremental and does not have the disadvantages of classic, monolithic LTO (i.e., memory requirements, not incremental-build friendly) nor of LIPO (i.e., compile/profiling time). ThinLTO does not combine the bit code of all modules into a monolithic bit code module. Instead per-function summaries are generated and the summary info is linked into a global index. LTO is performed in parallel for all modules and only for modules in their dependent module list (i.e., in monolithic LTO all modules are combined). However, this approach requires multi-threaded linking and therefore a specific linker tool.

### 2.3 Ultra-Low Power Software

There exist various code compression techniques to reduce the instruction memory footprint of embedded processors. The basic idea is to store a compressed version of the machine instructions in memory and decompress them during instruction fetch. In asymmetric compression methods, the code is compressed in software and decompressed by hardware. There is no need to change the CPU or compiler, but an additional HW decompression block is required that may penalize performance. The block may either be located before or behind the instruction cache, which then either holds decompressed original instructions or the compressed instructions. With this, [13] achieved 74% compression ratio for MIPS cores using Huffman codes. Using V2FCC, [14] reached 68-84% compression ratio for the VLIW processor TMS320C6x. [15] proposed dictionary-based code-compression. The basic idea is to look for the most used instruction words and encode these into the shortest code words. Decompression is relatively simple but the dictionary must be counted as additional hardware overhead. [16] describes bitmask-based code compression. It additionally exploits that symbols next to each other in the dictionary are often similar by defining a bitmask with position and difference. The field is still actively studied, e.g. [17] proposed separated dictionaries recently to improve performance and power use. For commercial solutions, e.g., for IBM's CodePACK tool a compression ratio above 60% was reported for PowerPC [18]. Some compression techniques can also directly be implemented in the compiler and do not require hardware modifications [63]. If the hardware can be tailored to a specific piece of software, it is also possible to adjust the ISA in order to reduce redundancies [64]. Some tools have been developed to explore the code compression design space [65, 66].

There exist many ways to reduce the memory footprint by writing efficient source code and applying source-code-level best practices. These may include stringent use of *const* declaration on constants and look-up tables, careful allocation of stack memory, compressed data structures, or use of unions and bit fields. Another way is to generate the source code based on a configuration. An example is Infineon's DAVE Tool that can generate the SW for the XMC controller family.

The arrival of artificial intelligence (AI) applications to IoT devices has brought considerable challenges to IoT device memory needs. Convolutional Neural Networks (CNNs) present the cutting-edge paradigm in AI technologies, but require by default huge amounts of memory to operate. To this end, many papers are addressing memory footprint reduction for CNN computation with CPUs or accelerators in the recent years. One of the most promising approaches is the binarization of CNNs, which reduces the memory need of a CNN to 1/30 of the original [86]. Another very specific approach utilizing generation for obtaining optimized results is described in [83]. Here, an optimized mapping of quadratic programs for embedded is described.

Another aspect is addressed in [82]. Here, the benefit of heterogeneous multi-core architectures for smaller memory footprints is addressed. To generalize these statements, digital blocks can be used to reduce memory footprint as well.

In addition to code compactness, care should be given for efficient data handling. Raw data should be processed as early as possible, computing efficiency permitting, to reduce need to transmit or store redundant information. The information could also be truncated to remove unnecessary detail, e.g., noise, above spec accuracy. When performing calculations, efficient algorithms should be used with emphasis on keeping the working set in either local scratch memory or in a write-back configured data cache, if present. This recommendation is to avoid spending energy on hitting the system memory bus.

Many small processors include data processing DSP or SIMD extensions, e.g., Xtensa HIFI extensions, ARM Cortex-M4/M33/M7 DSP extensions, or the upcoming RISC-V V extension. These usually are more optimized for data processing than regular computing engines. Using these does often require extra programming effort due to restrictions on data types or the need to invoke the intrinsics directly, because compilers lack the support to use these automatically.

Unless the data processing is time-critical, it would be prudent to reduce the clock frequency and voltage. Though this would increase the compute time, the overall energy per calculation would decrease. However, using this technique does require some hardware support.

The downside of these approaches is that designers apply them independently and without consideration of the specifics of the hardware platform or scenario in which the node is used. Here COMPACT tries to combine several approaches and generate code that applies best practices for minimizing memory footprints as well as code that enables compiler and compression techniques.

## 2.4 IoT Security

In most IoT scenarios, ultra-thin IoT devices communicate with each other and/or some form of infrastructure, e.g., servers over the Internet. In this context, IoT security means, ultimately, the protection of data against untrusted parties. Commonly, there are three forms of data that need to be protected: data in motion, data in use, and data at rest.

While protecting data in use is an important goal on its own, achieving meaningful results on IoT devices is difficult without special processors and memories. This type of hardware is only available in very high-end solutions and thus unlikely to be used in a typical IoT device. Similarly, protecting data at rest in an IoT device has its challenges: protecting sensitive data stored in a ROM against invasive attacks requires special memories, which again adds cost. To target the largest class of IoT devices – those, which do not have extra security hardware – the focus is on protecting data in motion, i.e., data that is transmitted between IoT devices or between an IoT device and a server. To this end, two principal modes of attack are assumed: A would-be attacker intercepts or eavesdrops on data as it is transmitted to read or modify it. Alternatively, the attacker may use public communication interfaces of IoT devices or servers to try to gain knowledge of sensitive data.

Protecting data in motion against the above-mentioned attacker requires strong cryptography to assert integrity, confidentiality, and authenticity of data (or a subset of these attributes). Protecting interfaces requires ensuring that all program code that handles interactions with the public (i.e., the Internet) is free from logic and programming errors which could be exploited. While achieving bug-free software is still considered impossible, exposed code can be significantly hardened by manual/semi-automatic code reviews. Another class of attack on interfaces that needs to be prevented are so-called side-channel attacks. Consistent with the attacker model outlined above, we consider only such channels that can potentially be executed via the Internet, e.g., timing side-channels. These attacks aim to extract cryptographic secrets to break encrypted communication; the best countermeasure is to make sure that all cryptographic code is timing invariant.

Protecting data in motion over the Internet is commonly achieved via TLS (Transport Layer Security) [33]. However, for the IoT scenario (where computational power is low) alternatives have been developed such as Datagram TLS (DTLS) [34], HIP Diet EXchange (DEX) [35], and minimal IKEv2 [36]. All three of them propose the usage of public key cryptography for key agreement and entity authentication. Only DTLS optionally defines a symmetric key based key agreement scheme. On the other hand, techniques from WSNs (Wireless Sensor Networks) are adapted to the context of IoT. As an example, a very low cost symmetric key based solution has been proposed in [37], [38] to secure a home automation system. The solution is based on the SPINS scheme [39] and ZigBee symmetric key agreement protocol [40].

Protecting public interfaces against the exploitation of software problems has a relatively long history, with most the research targeting PC-based systems. Commercial tools such as Klocwork [41] or Coverty [42] automatically validate that program code (such as C, C++) conforms to a given standard, e.g., MISRA-C. These tools furthermore greatly simplify the manual analysis of code.

The protection of cryptographic code against timing side-channels came into the spotlight after an academic attack on the RSA algorithm [43]. Later, more research has been performed with the goal of preventing such attacks; the idea was to write code such that the timing behaviour is independent of any sensitive data (e.g., key material). Lately, instead of programming standard algorithms in a specific way—thus artificially slowing down already complex algorithms—a new set of cryptographic algorithms was developed which is inherently resistant to timing attacks [44]. Work is now ongoing to incorporate these algorithms into standards such as TLS and DTLS. Finally, to ensure that code carefully written in C (or C++) is not transformed into non-constant code by the compiler, recent work has focused on statistically measuring the timing behaviour of machine code [45].

## 2.5 IoT Operating Systems

There exists a range of Operating Systems (OS), usually, with real-time capabilities (RTOS), for the embedded and IoT domain. These Operating Systems are developed for resource constraint devices and usually provide options for feature customizations. For example, TinyOS is an open source BSD licensed OS for low power wireless embedded system such as sensor node-type IoT devices [19]. Similarly, Zephyr OS is another open source RTOS, managed by the Linux foundation. It supports multiple architectures and targets connected resource-constrained IoT devices [20]. RIOT OS is another open source project. The RIOT OS runs on several platforms including embedded devices and PCs. Its greatest advantage is an easy-to-use API. It targets power efficiency and has low resource demand [21]. A commercial RTOS solution is VxWorks from Intel Windriver [22]. It is a modular OS that can be configured for embedded target devices. Another commercial solution is Mentor's Nucleus RTOS [23]. It also offers a rich feature set for embedded devices. eCos is an embedded operating system supporting a large number of target architectures and platforms [24]. It is highly configurable to enable its adaptation for a particular application. For example, it can be configured to support the POSIX thread API or to enable/disable support for task pre-emption in the scheduler. Over 200 such, partially inter-dependent, options are available [25]. Most recently, ERIKA Enterprise became popular in the automotive domains. ERIKA Enterprise is an open-source OSEK/VDX (AUTOSAR) hard real time OS with 1 - 4KB flash footprint and multi-core and stack sharing support [85].



Compared to the software adaptation envisioned by COMPACT, there are two main limitations: First, even though a large number of configuration options is offered, the level of configurability is well below what is possible in principle. For example, peripheral drivers can be included or excluded, but the same is usually not possible for individual driver features. Second, configuration options have to be set manually by an expert even if they could potentially be selected automatically. For example, the POSIX thread API could be enabled/disabled automatically by detecting if API calls are called by an application. The effort required to choose such options also limits the number of options that can be offered efficiently. HIPPEROS Tiny is a minimalist version of the HIPPEROS RTOS family designed specifically for IoT devices (Class 1 or Class 2) [26].

## 2.6 GPU Code Generation and Optimization

Graphics Processing Units (GPUs) are the prevailing programmable accelerator concept for speeding up AI applications on IoT devices as well as in mobile computing. NVidia has a strong hold of desktop and server GPU hardware for AI related computing. This is mainly due to the advanced level of software interfaces it provides for the user. Specifically, the CuDNN middleware (and the CUDA compiler architecture) is designed for speeding up computationally intensive AI computations. For example, CuDNN offers NVidia hardware optimized implementations of convolution and matrix multiplication, which form the majority (>90%) of computing time used by the device. Outside the NVidia ecosystem, the OpenCL language is the only competitor. The benefit of OpenCL is its larger range of available platforms and vendors, including embedded, desktop and cloud enabled hardware.

Current research on automatic code optimization for GPUs is largely focused on the OpenCL programming model [56]. However, due to its generality and device type independence, the common platform model it presents poses some limitations in exposing the particular features of each GPU platform, resulting in multiple vendor specific extensions or several versions of the same program, costing extra working hours of programmers [57] [60]. Automatic code optimization is therefore essential to lower the cost of using GPU platforms for general computing.

Research on GPU code optimization focuses on two aspects that significantly differ between platforms: parallelism granularity and the memory model [58]. Jääskeläinen et al. [57] propose an optimizing OpenCL kernel compiler. The compiler, which works at the LLVM IR level, starts by extracting data parallelism information from the OpenCL kernels in a device independent phase. This information is then compiled in a target dependent manner which supports several types of fine grained parallel resources, such as SIMD extensions, SIMD data paths and static multi-use. Shen et al. [58] focus on code transformations for OpenCL performance portability, which, despite being aimed at CPU target platforms, are also of interest when targeting different types of GPU architectures. The proposed transformations, which can be applied in an automated way by a source to source compiler, include tiling for increased cache-locality, selection between implicit and explicit vectorization, adaptation of the memory access patterns depending on the support for coalesced memory accesses and work-group size selection for optimal trade-off between scheduling overhead and flexibility. Daga et al. [59] identify a series of target specific optimizations that can be implemented at compile time which include: mitigation of divergent executing, selective loop unrolling and automatic vectorization. Divergent execution paths affect different architectures differently, depending on the total number of cores handled by each single scheduler. One proposed method to avoid divergence is to use kernel splitting, separating different branches into different kernels. This solution is useful when the conditional value can be determined before to the kernel launch, in which case the required branch can be automatically selected by the scheduler. Another proposed optimization is loop unrolling that accounts for the target memory architecture. Here the authors propose that in some cases, it might be beneficial to leave memory accesses vectorized while unrolling only the computational elements. Finally, the use of vector types for computation, as opposed to scalar types, can also lead to significant performance gains in platforms sporting VLIW architecture, both by increasing the computational unit usage and lowering the dynamic instruction count. All these transformations, either at source level or intermediate level can be introduced in an optimizing kernel compiler which is aware of different hardware architectures and transforms the parallel regions accordingly, such as pocl [57]. However, combining different optimizations must be done with care, as not all of them are orthogonal [59],

as, for example, the increase of register pressure might lead to a reduced total number of simultaneous threads. Finally, because of its general nature and the problems faced when supporting very different GPU architectures, optimizations designed for OpenCL code can be applied to other GPU programming models, such as NVIDIA's CUDA.

The inconvenience that programming of (embedded) GPUs is done by both the CUDA and the OpenCL language is alleviated by Halide [87], a high-level functional language that has a compiler that can produce executables for both CUDA and OpenCL enabled devices. Another benefit of Halide is that the language decouples the functional description of algorithms from the scheduling of the algorithms' operations, which makes Halide algorithm descriptions very portable, ranging from regular CPUs to DSPs and GPUs.

## 2.7 IoT Analysis

The COMPACT analysis framework is mainly based on Virtual Prototyping platforms, which are integrated development environments. They provide the means to model, simulate, analyse, and verify heterogeneous mixed software/hardware system models. In the context of Electronic System Level (ESL) design, the notion of Virtual Prototyping mainly refers to the execution of target compiled software binary on hardware models before the final hardware is available.

Through the last years, virtual prototyping platforms based on Just-in-Time compilation became quite popular as they provide a significantly faster execution speed than cycle-accurate simulators. Popular commercial virtual prototyping environments are the Cadence Virtual System Platform [48], Mentor Graphics Vista [49], Synopsys Virtualizer [50], and Intel Simics [51]. QEMU [52], and OVP [53] are comparable widely accepted and freely available platforms with a high stability and speed.

The different tools mainly vary in the features of their integrated development environments and in the supported hardware modelling language. COMPACT will apply some of those Virtual Prototyping Environments and also plans to contribute to the open source process with new enhancements with focus on QEMU for configurable RISC-V platforms. For this IoT-specific analysis concepts and model generated test benches are investigated.

Besides the execution of target binary code in a simulator, approaches exist that allow timing simulations by execution of timing-annotated software directly on the simulation host, often referred to as source level simulation. This approach is also capable for virtual prototyping and offers even faster simulations than binary level simulators with only little less accuracy [61, 62].

For analysis of ultra-thin software, various open source and commercial solutions already exist, such as Valgrind, mtrace or many others. Not all can handle arbitrary embedded devices, as they have usually no understanding of the underlying hardware. COMPACT will here make sure that detailed analysis is available for ultra-thin IoT devices.

### 3 Related Projects

Project Name	Cooperative Programme	Time period (approx.)	Technical Focus	Relationship
HEADS	FP7	2013-2017	MDE approach, Heads/ThingML modelling language and tool-chain, Kevoree dynamic runtime management	No focus on ultra-thin IoT nodes, missing modelling view for ultra-thin devices
AMALTHEA/ AMATHEA4public	ITEA2 Call4/ ITEA2 Call8	2011-2014/ 2014-2017	Modelling applications, Engineering embedded multi- and many-core software systems	Focus on multi-cores, not on ultra-thin IoT nodes Investigation on re-using application meta-models
MACH	ITEA2 Call7	2013-2016	Hybrid and embedded high performance computing systems	Focus on HPC, FZI will use MACH DS(e)L concepts and prototype tools for the efficient generation of target software.
REVaMP <sup>2</sup>	ITEA3 Call2	NA	Automation toolchain for Round-trip Engineering and Variability Management Platform and Process	Focus on legacy software and not on code optimization FZI will reuse tools developed to achieve an understanding of the target software as well as for verifying the generated COMPACT code.
ASSUME	ITEA3 Call1	2015-2018	Development methodology for affordable and safe multi-core systems	Focus on static safety analysis and safe code generation, not on efficient code for ultra-thin hardware. FZI will reuse ASSUME methods for the safety assessment of the generated target software by COMPACT tools
EMPHYSIS	ITEA3 Call2	NA	Methods to improve production code of embedded control systems in automotive vehicles, physical models of environment	Focus on control system performance, no special methodology for ultra-thin resource constraint devices
OPEES	ITEA2 Call3	2009-2012	Open Platform for the Engineering of Embedded Systems	No focus on IoT and networking

PARFAIT	ITEA3 Call2	NA	Personal data protection in the IoT domain, privacy and security framework	No focus on resource constraints, QoS and interoperability
ARMOUR	H2020	2016-2018	Large Scale Experiments of IoT Security Trust: A platform containing suitable duly tested solutions to cope with security, privacy and safety will be implemented and analysed.	No focus on interoperability or balance with QoS is made.
EBBITS	FP7	2010-2015	Service oriented architectures and technologies for IoT based on open protocols and middleware	Focus on global IoT infrastructure, no focus on IoT terminal nodes and edge devices
OPENES	CATRENE	2013-2016	Open ESL Technologies for Next Generation Embedded Systems	Model driven system design flow integrating functional and extra functional requirements
CRAFTERS	ARTEMIS	2012-2015	ConstRaint and Application driven Framework for Tailoring Embedded Real-time Systems	Address security and power aspects, but no focus on IoT and networking
VERDE	ITEA2	2009-2012	Verification-oriented design of embedded system	Component-based, model-driven design but no focus on resource-constrained systems and efficient application software generation
CONTREX	FP7	2013-2016	Design methods for mixed-criticality embedded system design with consideration of extra-functional properties	CONTREX can provide background technology for mixed-criticality embedded systems to be extended whenever useful to the IoT domain

**Table 1: Related collaborative research projects.**

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## 5 Appendix A - Table of Acronyms

Acronym	Definition
AADL	Architecture Analysis and Design Language
ARM	Advanced RISC Machine
ASIC	Application Specific Integrated Circuit
BIP	Behaviour, Interaction, Priority
BSD	Berkeley Software Distribution
COMPACT	Cost-efficient Smart System Software Synthesis
CNN	Convolutional Neural Networks
CPU	Central Processing Unit
CVL	Common Variability Language
DSP	Digital Signal Processor
DTLS	Datagram Transport Layer Security
EAST-ADL	Electronics Architecture and Software Technology - Architecture Description Language
EDA	Electronic Design Automation
ESL	Electronic System Level
FODA	Feature-Oriented Domain Analysis
FPGA	Field-programmable Gate Array
GPU	Graphics Processing Unit
IoT	Internet of Things
IoT-PML	Internet of Things Platform Modelling Language
IPO	Inter-procedural Optimization
ISA	Instruction Set Architecture
IR	Intermediate Representation
IVML	INDENICA Variability Modeling Language
LIPO	Light-weight Inter-procedural Optimization
LLVM	Low Level Virtual Machine
LTO	Link Time Optimization
MDA	Model Driven Architecture
MDE	Model Driven Engineering
MIPS	Mega Instructions Per Second
OMG	Object Management Group
OVP	Open Virtual Platforms
PGO	Profile Guided Optimizations
POSIX	Portable Operating System Interface
QEMU	Quick Emulator
RAM	Random Access Memory
REST	Representational State Transfer
RISC	Reduces Instruction Set Computer
ROM	Read Only Memory
RSA	Rivest-Shamir-Adleman
RTOS	Real Time Operating System
RVC-CAL	Reconfigurable Video Coding – Cal Actor Language
SoC	System on Chip
SIMD	Single Instruction, Multiple Data
SysML	Systems Modelling Language
TLS	Transport Layer Security
TTA	Transport Triggered Architecture
UML	Unified Modeling Language
UPDM	Unified Profile for DoDAF/MODAF
VLIW	Very Long Instruction Word
VSL	Variability Specification Language
V2FCC	Variable-to-fixed Code Compression